CND 221: Digital Testing and Verification

Course Description

The main objective of this course is to cover the verification tools and methods, with emphasis on SystemVerilog, for digital circuits and systems with a focus on formal Hardware verification techniques. The course will cover both conventional and advanced formal tools, algorithms, and technologies that are employed to verify such implementations as core computational platforms. The circuit verification includes two- or multi-level verification, model-checking simulation-based, and automatic test-pattern-generation-based-verification.

Prerequisites
Introduction to Digital Design

Learning Outcomes
After successful completion of this course, the student will be able to:
1. Define the relationship between fault models and physical failures,
2. Use SystemVerilog to describe and verify digital systems
3. Compute testing objectives from high-level descriptions.
4. Design efficient logic and fault simulators,
5. Generate relevant test patterns using different techniques
6. Distinguish various design-for-testability methods

Course Materials
- Mark Zwolinski, Digital System Design with SystemVerilog, Prentice Hall.
- N. K. Jha, S. Gupta, Testing of Digital Systems, Cambridge University Press
- Lun Li, Mitchell A. Thornton, Digital System Verification, A Combined Formal Methods and Simulation Framework, Springer

Course Schedule

- Introduction to digital Verification
- **SystemVerilog Object-Oriented Verification**
    - Introduction to SystemVerilog
    - Verilog and SystemVerilog Syntax and Semantics
    - Procedures, Programming Statements and Operators
    - SystemVerilog User-defined Types and Packages
    - SystemVerilog Interfaces
    - Using interfaces to simplify inter-module connections
    - Verilog Verification Constructs
    - Program Blocks and Clocking Domains
    - Object-oriented programming
    - Dynamic Arrays and Scoreboards
    - Process Synchronization
    - Constrained Random Value Generation
    - Functional Coverage
    - Overview of SystemVerilog Assertions
    - Assertion concepts
    - Overview of SystemVerilog UVM
- **Universal Verification Methodology**
    - UVM Overview
    - UVM First Look
    - UVM Sequence items and Sequences
    - UVM Sequencers and Drivers
    - UVM Monitors and Agents
    - UVM Functional coverage
    - UVM Environments, Predictors and Scoreboards
    - UVM Tests and Advanced Sequences
    - UVM Factory and UVM Configuration
    - UVM Register Layer Overview
- **Validation and test of manufacturing circuits**
    - Test Procedure
    - Design for Testability
    - Test-Pattern Generation
    - Fault Models
    - Automatic Test-Pattern Generation (ATPG)
- **Verification**
    - Testbench design and formal verification
    - On-Chip Verification
    - Physical Verification