CND 211: Advanced Full Custom VLSI Design

Course Description

The main objective of this course is to introduce the students to modern advanced full custom VLSI digital integrated circuits. The student will be introduced to the implementation strategies in digital IC design, dealing with timing issues. In addition, the interconnect modeling and spice wire model will be demystified. The students get hands-on experience in using modern industrial CAD tools.

Prerequisites

Introduction to Silicon Process and VLSI

Learning Outcomes

After successful completion of this course, the student will be able to:

1. Design advanced CMOS digital integrated circuits through a hands-on design process.
2. Practice designing arithmetic building blocks and memory structures using a full-custom design flow.
3. Cope with the interconnect, define its different aspects, and deal with its issues.
4. Dealing with the timing issues in digital circuits.

Course Materials

Textbook:

- Rabaey, Jan, Anantha Chandrakasan, and Bora Nikolic. Digital Integrated Circuits: A Design Perspective. 2nd ed. Prentice Hall.
- Johnson, Howard, Graham, Martin. High Speed Digital Design: A Handbook of Black Magic. Pearson.
- Weste, Neil, Harris, David. CMOS VLSI Design: A Circuits and Systems Perspective 4th Ed. Pearson.
- Material is also derived from the IEEE Journals, Transactions, and flagship Conference proceedings.

Course Topics and Schedule

- Implementation strategies for digital ICs
  - From Custom to Semi-custom and Structured Array Design Approaches
  - Custom Circuit Design
  - Cell-Based Design Methodology
  - Array-Based Implementation Approaches
- Coping with interconnect
  - Capacitive Parasitics, Resistive Parasitics, Inductive Parasitics, and Advanced Interconnect Techniques
- Timing issues in digital circuits
  - Timing Classification of Digital Systems
  - Synchronous Interconnect
  - Synchronous Design — An In-depth Perspective
  - Self-Timed Circuit Design
  - Synchronizers and Arbiters
  - Clock Synthesis and Synchronization Using a Phase-Locked Loop
- Designing arithmetic building blocks
  - Datapaths in Digital Processor Architectures
  - The Adder, Multiplier, Shifter, and Other Arithmetic Operators
  - Power and Speed Trade-off in Datapath Structures
- Designing memory and array structures
  - The Memory Core
  - Memory Peripheral Circuitry
  - Memory Reliability and Yield
  - Power Dissipation in Memories
  - Case Studies in Memory Design
- Interconnect Modeling — Capacitance, Resistance, and Inductance, Electrical Wire Models
  - SPICE Wire Models