CND 201: Advanced Digital Design

Course Description

The main objective of this course is to introduce the students to advanced digital integrated circuit design with emphasis on "hands-on" digital IC design using modern CAD tools. The student will be introduced to the digital design flow for both FPGA and ASIC including Verilog modeling, synthesis, timing analysis and constraints, clock synthesis, placement and routing, signal and power integrity issues, and design for testing.

Prerequisites

Introduction to Digital Design

Learning Outcomes

After successful completion of this course, the student will be able to:

1. Learn the full cycle of design of digital IC starting from defining specifications, functional design, design, and layout to build a cell library.
2. Know how to use modern industrial EDA design tools to perform advanced circuit design.
3. Learn how to build and optimize algorithms to run very quickly on custom hardware.

Course Materials

- Wayne Wolf, "Modern VLSI Design" Prentice-Hall, 4th Edition, 2008.
- Givanni De Micheli, "Synthesis & Optimization of Digital Circuits". McGraw Hill, 2003.
- Vaibbhav Taraate. Logic Synthesis and SOC Prototyping RTL Design using HDL. Springer
- Rabaey, Jan, Anantha Chandrakasan, and Bora Nikolic. Digital Integrated Circuits: A Design Perspective. 2nd ed. Prentice Hall.
- Weste, Neil, Harris, David. CMOS VLSI Design: A Circuits and Systems Perspective 4th Ed. Pearson.
- Material is also derived from the IEEE Journals, Transactions, and flagship Conference proceedings.

Course Topics and Schedule

- Digital design flow
- Verilog
    - Behavioral modeling
    - Structural modeling
- RTL design
- FPGA architecture
- ASIC Physical Design
- Introduction to Physical Design Flow
- Logic Synthesis
- Timing and Area Constraints
- Design for Test
- Attributes and Constraints
- Compile Strategies
- Physical Design Data
- Design Planning
- Placement
- Clock Tree Synthesis
- Routing
- Power Optimization
- Static Timing Analysis
- Signal and Power Integrity